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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,666	09/18/2003	Douglas R. Hackler SR.	51889/5	4619

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EXAMINER	
THOMAS, ERIC W	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,666	HACKLER ET AL.	
	Examiner	Art Unit	
	Eric W. Thomas	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-12,26-38 and 55-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-12,26-38,55-60 and 62-64* is/are rejected.

7)☒ Claim(s) *61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/18/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

INTRODUCTION

The examiner acknowledges, as recommended in the MPEP, the applicant's submission of the amendment dated 6/30/05. At this point, claims 1, 26 have been amended; claims 8, 13-25, 39-54 have been cancelled; and claims 55-64 have been added. Thus claims 1-7, 9-12, 26-38, 55-64 are pending in the instant application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6-7, 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Delpech et al. (US 2003/0213989).

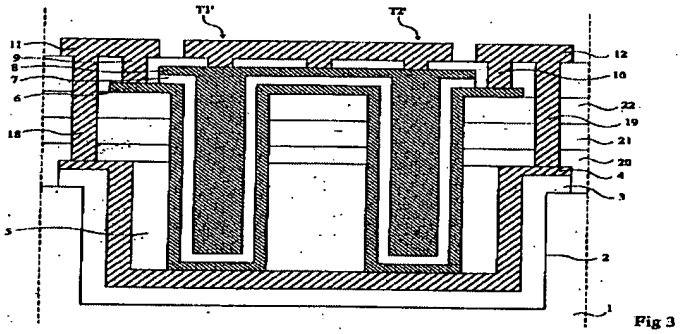


Fig 3

Delpech et al. disclose in fig. 3, a substrate (1), a conductive material (4) formed above the substrate; an insulating material (5, 20-22) formed on the conductive material wherein the insulating material and the conductive material serve as a form for defining a plurality of capacitor trenches above the conductive layer, the insulating material defines the trench sidewalls and the conductive material defines the trench bases, a bottom electrode (6) formed onto the capacitor trenches so as to form a layer within the capacitor trenches in contact with the conductive material, wherein the bottom electrode extends up the sides of the capacitor trenches to form bottom electrode sidewalls; a capacitor dielectric (7) at least partially positioned on the bottom electrode; and a top electrode (7) at least partially positioned on the capacitor dielectric, and completely filling the capacitor trenches.

Regarding claim 2, Delpech et al. disclose the capacitor dielectric (see paragraph 41 – Ta_2O_5) is made from a material having a higher dielectric constant than the dielectric constant of the insulating material (SiO_2 – see paragraph 37)

Regarding claim 3, Delpech et al. disclose the capacitor dielectric has a high-k dielectric constant (paragraph 41).

Regarding claim 4, Delpech et al. disclose the capacitor dielectric has a dielectric constant greater than or equal to about 6.0 (see paragraph 41 – Ta_2O_5).

Regarding claim 6, Delpech et al. disclose the capacitor structure is a discrete capacitor.

Regarding claim 7, Delpech et al. disclose the capacitor structure is configured to be part of an integrated circuit (paragraph 2).

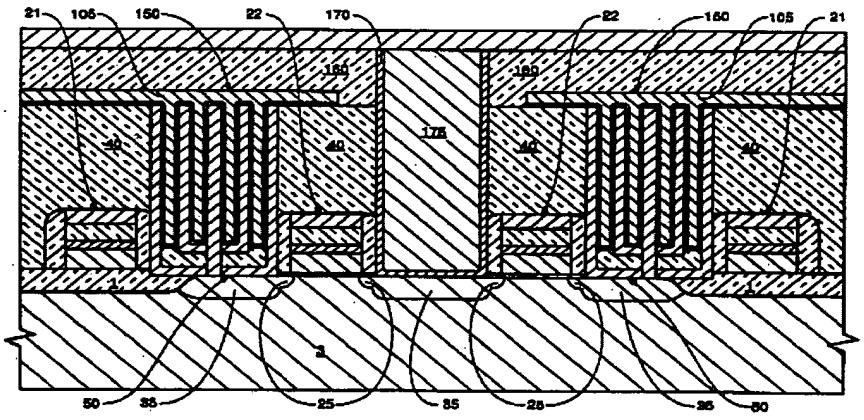
Regarding claim 9, Delpech et al. disclose the conductive material layer is comprised of a different material than the bottom electrode (paragraphs 35 & 40).

Regarding claim 10, Delpech et al. disclose the top electrode is disposed in the capacitor trenches such that the top electrode interdigitates with the bottom electrode.

Regarding claim 11, Delpech et al. disclose the bottom electrode further comprises a bottom electrode top wall (see fig. 3).

Regarding claim 12, Delpech et al. disclose the bottom electrode further comprises a bottom electrode base (see fig. 3).

3. Claims 26-29, 31-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Gonzalez et al. (US 5,150,276).



Gonzalez et al. disclose a capacitor structure comprising: a substrate (3), an insulating material (40) formed on the substrate, wherein the insulating material serves as a form for defining a capacitor trench; a bottom electrode (60, 86), wherein the bottom electrode comprises a bottom electrode layer (60) in the capacitor trench and a bottom electrode plug (86) disposed in the capacitor trench, wherein the bottom

electrode layer extends up the sides of the capacitor trench to form bottom electrode sidewalls; a capacitor dielectric (100) at least partially position on the bottom electrode and in direct contact with the bottom electrode plug formed around a majority of the bottom electrode plug; a top electrode (105) formed around a majority the bottom electrode plug.

Regarding claim 27, Gonzalez et al. disclose the capacitor dielectric is made from a material having a higher dielectric constant (silicon nitride) than the dielectric constant of the insulating material (BPSG).

Regarding claim 28, Gonzalez et al. disclose capacitor dielectric has a high-k dielectric constant (silicon nitride).

Regarding claim 29, Gonzalez et al. disclose the capacitor dielectric has a dielectric constant greater than or equal to about 6.0 (silicon nitride).

Regarding claim 31, Gonzalez et al. disclose the capacitor structure is a discrete capacitor.

Regarding claim 32, Gonzalez et al. disclose the capacitor structure is configured to be part of an integrated circuit.

Regarding claim 33, Gonzalez et al. disclose a conductive material layer (35), wherein the conductive layer is in contact with the bottom electrode.

Regarding claim 34, Gonzalez et al. disclose the conductive material layer is a different material than the bottom electrode.

Regarding claim 35, Gonzalez et al. disclose the bottom electrode and the capacitor dielectric are formed in the shape of a box (abstract and fig. 7b, 9a).

Regarding claim 36, Gonzalez et al. disclose the top electrode is a least partially disposed in the capacitor trench such that the top electrode interdigitates the bottom electrode.

Regarding claim 37, Gonzalez et al. disclose the bottom electrode further comprises a bottom electrode top wall.

Regarding claim 38, Gonzalez et al. disclose the bottom electrode further comprises a bottom electrode base.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Delpech et al. (US 2003/0213989) in view of Alers et al. (US 6,320,244).

Delpech et al. disclose the claimed invention except for the capacitor dielectric is formed from a stack comprising more than one material.

Alers et al. teach that it is known in the capacitor art to form a dielectric layer from a stack of dielectric materials having more than one material.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the dielectric of Alers et al. in the capacitor of Delpech et al, since such a modification would provide a high quality dielectric having a high dielectric constant and low leakage.

7. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez et al. (US 5,150,276) in view of Alers et al. (US 6,320,244).

Kubo discloses the claimed invention except for the capacitor dielectric is formed from a stack comprising more than one material.

Alers et al. teach that it is known in the capacitor art to form a dielectric layer from a stack of dielectric materials having more than one material.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the dielectric of Alers et al. in the capacitor of Kubo, since such a modification would provide a high quality dielectric having a high dielectric constant and low leakage.

8. Claims 55-60, 62, 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delpech et al. (US 2003/0213989) in view of Gonzalez et al. (US 5,150,276).

Delpech et al. disclose in fig. 3, a substrate (1), a metal layer (4) formed above the substrate; an insulating material (5, 20-22) formed on the conductive material

wherein the insulating material serves as an outside wall for defining a capacitor trench above the metal layer; a bottom electrode (6) formed in the capacitor trench wherein the bottom electrode directly contacts the metal layer and extends up the sides of the capacitor trench to form bottom electrode sidewalls; a capacitor dielectric (7) at least partially positioned on the bottom electrode and in direct contact with the bottom electrode layer; and a top electrode (7) at least partially positioned on the capacitor dielectric.

Delpech et al. disclose the claimed invention except for the bottom electrode comprises a bottom electrode plug disposed within the capacitor trench, and the capacitor dielectric in direct contact with the bottom electrode plug.

Gonzalez et al. teach that it is known in the capacitor art to form a bottom electrode from a bottom electrode layer and a bottom electrode plug; wherein the dielectric layer directly contacts that bottom electrode layer and the bottom electrode plug. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom electrode of Delpech et al. having the same structure as the electrode of Gonzalez et al., since such a modification would produce an electrode having high surface area.

Regarding claim 56, the modified Delpech et al. disclose the bottom electrode plug is disposed between the bottom electrode layer and the capacitor dielectric such that the bottom electrode plug is in indirect contact with the metal layer (Gonzalez et al. teach that the bottom electrode plug is disposed between the bottom electrode layer and the capacitor dielectric – see fig. 12A).

Regarding claim 57, the modified Delpech et al. disclose the bottom electrode plug is completely disposed within the capacitor trench and extends approximately the same length as the outside sidewall.

Regarding claim 58, the modified Delpech et al. disclose the bottom electrode plug includes a metal (See Delpech et al. paragraph 40).

Regarding claim 59, the modified Delpech et al. disclose the capacitor dielectric and the top electrode extend around a majority of the bottom electrode plug.

Regarding claim 60, the modified Delpech et al. disclose an insulating plug formed on the metal layer and defining inside sidewalls for the capacitor trench, wherein the bottom electrode layer, the capacitor dielectric, and the top electrode layer at least partially extend around the insulating plug (see fig. 6).

Regarding claim 62, the modified Delpech et al. disclose the capacitor dielectric has a dielectric constant greater than or equal to about 6.

Regarding claim 64, the modified Delpech et al. disclose the bottom electrode layer further comprises a bottom electrode top wall.

9. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Delpech et al. (US 2003/0213989) and Gonzalez et al. (US 5,150,276) as applied to claim 55 above, and further in view of Alers et al. (US 6,320,244).

Delpech et al. disclose the claimed invention except for the capacitor dielectric is formed from a stack comprising more than one material.

Alers et al. teach that it is known in the capacitor art to form a dielectric layer from a stack of dielectric materials having more than one material.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the dielectric of Alers et al. in the capacitor of Delpech et al, since such a modification would provide a high quality dielectric having a high dielectric constant and low leakage.

Allowable Subject Matter

10. Claim 61 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or fairly suggest (taken in combination with the other claimed features) a capacitor comprising a second bottom electrode plug disposed within the capacitor trench (claim 61).

Response to Arguments

12. Applicant's arguments with respect to claims 1-7, 9-12, 26-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W. Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on Monday - Friday 5:30 AM - 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric W Thomas
Primary Examiner
Art Unit 2831

ewt

ERIC W. THOMAS
PRIMARY EXAMINER